UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/764,803	01/26/2004	Payman Zarkesh-Ha	02-5938	9749

24319 7590 12/11/2006

LSI LOGIC CORPORATION
1621 BARBER LANE
MS: D-106
MILPITAS, CA 95035

EXAMINER	
KIM, SU C	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 12/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/764,803	ZARKESH-HA ET AL.	
	Examiner	Art Unit	
	Su C. Kim	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 January 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

HSIEN-MING LEE
PRIMARY EXAMINER

12/4/06

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/26/04,2/15/06,7/06/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of Species I (Claims 1-24) in the reply filed on 9/8/2006 acknowledged. The Examiner withdraws the previous Election /Restriction requirement after further consideration of the instant application.

Claim Objections

2. Claim 22 is objected to because of the following informalities: "poly layer" is unclear please define poly layer as poly silicon layer or multiple layers?

The examiner now considers any "poly layer" as poly silicon layer until applicant clarify what poly layer means.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1- 5, 7-13, 15, &16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Byrn et al. (US 6910201) in view of Adachi et al. (US 20020072135)

Regarding claims 1 & 9, Byrn discloses a method for providing field programmable platform array units (any programmable units are considered as field programmable units), comprising:

Cutting N by M (Fig. 2A) array of platform array units from a field programmable platform array wafer (Fig. 2A, 130) according to an order from a customer (every chip is ordered by a customer or customers), N and M being positive integers, said field programmable platform array wafer having all silicon layers (column 2, lines 1-12) and metal layer (column 5, lines 30-40) built and including a plurality of platform array unit (Column 6 lines 20-25, the unit has a plurality of circuit layers), said plurality of platform array units being field programmable by a customer (column 4, lines 36-48) including core(Fig. 2B, chip) and one processor (Fig. 2B, logic element) and interconnect (column 5, lines 30-40) between plurality of platform array units being pre-routed on chip (Fig. 2B, 132)

Byrn fails to teach packaging and test N by M array of platform array units at the end of process.

Adachin suggests packaging and testing after dicing (Fig. 8)

Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant(s) claimed invention is made to provide Byrn with packaging and test N by M array of platform array units at the end of process taught by Adachin in order to reduce manufacture's defect.

Pertaining claims 2 &10, as applied to claims 1 & 9 above, Byrn and Adachi in combination discloses all the limitations include, programming N by M array of platform array units by customer (column 1 lines 56-67)

Pertaining claims 3 & 11, as applied to claims 2 &10 above, Byrn and Adachi in combination discloses all the limitations include, programming is performed for at least

one of unit specialization, unit role assignment, and inter-unit communications (Byrn, Column 4, lines 49-56, customizing the gate array can be considered as programming inter-unit communications or unit role assignment. Also see Adachi fig. 3)

Pertaining claims 4 & 12, as applied to claims 2 &10 above, Byrn and Adachi in combination discloses all the limitations include, programming is performed with firmware (column 4, lines 49-56, to customize by software tool 200, a firmware has to be implanted also FPGA is field programmable gate array. Also see Adachi fig. 3)

Pertaining claims 5 & 13, as applied to claims 1 & 9 above, Byrn and Adachi in combination discloses all the limitations include, N by M array of platform array units are within a single platform (Fig. 2C, N by M array 132 are within a single platform 130 (wafer))

Pertaining claims 7 & 15, as applied to claims 5 & 13 above, Byrn and Adachi in combination discloses all the limitations include, a digital signal process (DSP) process (Adachi, paragraph 0041, in addition, FPGA can also includes application of DSP (digital signal process on page 4 line 2 of "Field-programmable gate array" defined by www.answers.com, please refers "DSP"))

Pertaining claims 8 & 16, as applied to claims 1 & 9 above, Byrn and Adachi in combination discloses all the limitations include, storing field programmable platform array wafer(Byrn, Fig. 2C, the data or program can be stored in silicon chip which is a part from the wafer)

5. Claims 6 & 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Byrn et al. (US 6910201) in view of Adachi et al. (US 20020072135) and further in view of Wall et al. (US 6507923)

Pertaining claims 6 & 14, as applied to claims 5 & 13 above paragraph 4, Byrn and Adachi in combination discloses all the limitations include, a single platform (FPGA)

However, Byrn and Adachi in combination fail to teach a single platform is a storage area network (SAN) platform.

Wall suggests a field programmable gate array (hereafter, FPGA, Fig. FPGA 94) has a trace support in a fiber channel storage area network (Column 13, lines 39-59).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant(s) claimed invention is made to provide Byrn and Adachi in combination reference with a single platform is a storage area network (SAN) plat taught by Wall in order to produce smaller packaging size.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 17,18, 21, 22, & 23 are rejected under 35 U.S.C. 102(b) as being anticipated by Lee et al. (US 6222212)

Pertaining claim 17, Lee discloses a semiconductor device comprising:

A plurality of platform array units being field programmable by a customer (Fig. 7, field programmable semiconductor device 700), each of plurality of platform array units including at leas one core (Fig. 7, 721,field programmable element) and at leas one processor (Fig. 7, the logic elements are considered as a processor);
Wherein interconnect between plurality of platform array units (Fig. 7, a plurality of array is logic element 711) being pre-routed (Fig. 7, pre-routed 741-746, Fig. 9A, circuitry including metal interconnection 913)

Pertaining claims 18,21,22, & 23, as applied to claim 17 above paragraph 6, Lee discloses all the limitations include, top aluminum pads of semiconductor device are used as a routing layer (Fig. 2A, column 5, lines 35-44, the first interconnect layer 21 is aluminum, copper, titanium tungsten, poly silicide selectively doped)

8. Claims 19 & 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (US 6222212) in view of Glen et al. (US 6962829)

Pertaining claims 19 & 20, as applied to claim 17 above paragraph 6, Lee discloses all the limitations include, metal plug (Fig. 7, 751-756) of semiconductor device are used as routing layer

However, Lee fails to teach metal bump structure of semiconductor device are used as routing layer with encapsulation of lower copper metal layers.

Glen discloses metal bump structure with copper metallization (Fig. 2, copper metallization 38, 22) with encapsulation of lower copper metal layers (Fig. 2, encapsulated the bump structure 18)

Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant(s) claimed invention is made to provide Lee reference with metal bump structure of semiconductor device are used as routing layer with encapsulation of lower copper metal layers taught by Glen in order to enhance bonding strength between chip and board.

9. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (US 6222212) in view of White. (US 20040068330)

Pertaining claim 24, as applied to claim 17 above paragraph 6, Lee discloses all the limitations include, plurality of platform array units (Fig. 7, 721-722)

However, Lee fails to teach configured by external software programming

White discloses updating FPGA by external software programming (paragraph 0004)

Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant(s) claimed invention is made to provide Lee reference with configured by external software programming taught by White in order to minimize time to programming and also reprogramming.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Su C. Kim whose telephone number is (571) 272-5972. The examiner can normally be reached on Monday - Thursday, 9:00AM to 7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Su C. Kim
12/5/2006

HSIEN-MING LEE
PRIMARY EXAMINER

12/7/06